Asynchronous FIFO / Double Synchronizer Description

The top-level instance generics C\_FIFO\_EXITST and C\_NUM\_TRANSFER\_BITS control whether the FIFO is generated and its width, or if a simple double synchronizer is generated. The depth of the FIFO modules will always be 16 elements. AXI and SPI interfaces will double synchronize non-data register values to their respective clocks.

The Tx FIFO handles AXI to SPI transactions. The data input is taken from the transmission data register. The write enable signal is controlled by the write response of the register module which indicates that valid data has been written to the register and can be passed to the FIFO. The read enable signal is controlled by the internal count of the serializer process in the SPI module requesting a new byte from the FIFO.

The Rx FIFO handles SPI to AXI transactions. The data output is sent to the receive data register. The read enable signal is controlled by the read response of the register module, indicating that the last register value has been read, and the next one can be loaded from the FIFO. The write enable signal is controlled by the internal count of de-serializer process in the SPI module indicating that the shift register is full.

Occupancy value and status flags are tied to the corresponding registers. The reset inputs are tied to the corresponding control register bits.